**Design of a 2W E -Band GaN MMIC Power Amplifier**

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## Introduction

Use of the mm-wave bands with inherent multi-GHz wide channel bandwidths, are crucial to enable the high-capacity, high-speed data transmission capabilities of next generation mobile and satellite communications networks. Recent improvements in available GaN foundry processes to achieve 0.1um gate geometries means that realising multi-Watt MMIC power amplifier solutions at E-band (60-90GHz) and W-band (90-110GHz) is becoming feasible. This work will cover unit cell characterisation, large signal modelling and simulation results for a 2W E-band MMIC power amplifier design at 71-76GHz.

## Choice of foundry process

On reviewing possible foundry options with E-band performance potential, the processes in Table1 were identified.

| COMPANY | MACOM (OMMIC) | NGC | WIN Semi |
|---|---|---|---|
| **PROCESS** | **D01GH** | **GAN09** | **NP12-01** |
| **TECHNOLOGY** | GaN/Si | GaN/SiC | GaN/SiC |
| **STATUS** | Production | Production | Production |
| **SPACE GRADE** | In process | - | - |
| **GATE LENGTH (nm)** | 100 | 90 | 120 |
| **THICKNESS (µm)** | 100 | 50 | 50 |
| **Ft(GHz)** | 110 | 100 | 40 |
| **Fmax(GHz)** | 180 | 250 | 150 |
| **Vbgd (V)** | 36 | | 120 |
| **Vds.q (V)** | 12 | 18 | 20-28 |
| **Idss (mA/mm)** | 1200 | - | 700 |
| **Idss MAX (mA/mm)** | 1700 | 1200 | 965 |
| **TRANSCONDUCTION (mS/mm)** | 800 | 525 | 415 |
| **MIM CAPACITORS (pF/mm²)** | 50 & 400 | - | 215 |
| **NOISE FIGURE (dB)** | 1.5 @ 40 GHz | - | - |
| **POWER DENSITY (mW/mm)** | 4000 | 2800 | 3400 |

*Table1.; Contender foundry processes for E-band operation*

PDK simulated performance together with commercial considerations were taken into account in selecting WIN Semiconductors 120nm GaN on SiC process as the candidate process.

Characterisation and Large Signal Model Implementation

Probed on-wafer S-parameters were carried out by Cardiff University to 110GHz on a number of sample unit cells with 2 and 4 fingers, and gate widths from 20 to 50um. Load pull was also carried out the unit cells at 16-28V and at frequencies 40GHz, 71GHz and 76GHz. The measurements were used to confirm the basic performance level at 76GHz and provided data for validating a large signal model.

For improved accuracy above 50GHz an in-house GaN HEMT model was used following the PI topology of Fig.1, with the core Ids current generator and Gate Source charge expressions based on Tajima's GaAs FET models. The nonlinear functions describing Ids and the charge sources are continuous and differentiable to provide both good convergence behaviour and the ability to appropriately handle IMD and harmonic responses. The model has been fitted to match primarily small signal S-parameters, (sample shown in Fig .2) with some input from DC and Large Signal data and is a first cut approach to assist with evaluating the large signal data and carrying out the HPA design work. Aside from a channel temperature sub model, second order items not critical to the model utility for the E-band project, such as drain source breakdown, forward gate current and trapping effects have not yet been included.

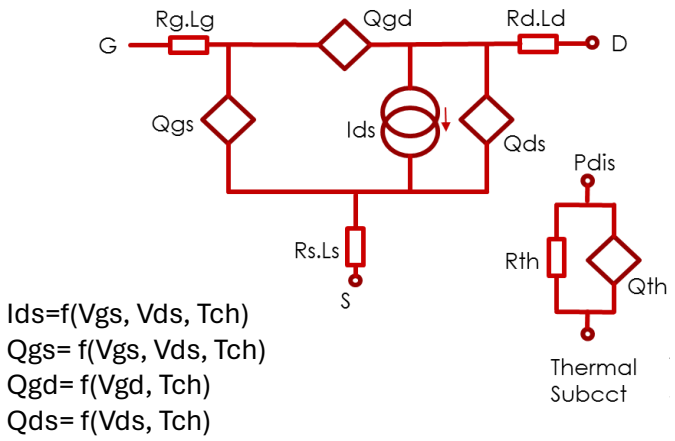


*Fig.1; The GaN HEMT Large Signal Model Topology, with Thermal Sub circuit*

An internal thermal sub circuit with a thermal resistance and capacitance allows a dynamic Tch variable to be calculated as a function of the instantaneous power dissipation. The thermal resistance in this case has been set to an estimated value, but can be fine tuned based on finte element simulation or measured values. The calculated Tch variable is applied to the internal nonlinear charge and current source functions to modify gain and power with temperature. The Temperature node can be

used to estimate the peak channel temperature under operation for reliability and lifetime assessment.

Trapping sub circuits can also be added to approximate gate and drain lag effects but were not deemed to be critical for the purposes of this project. Empirical evidence also suggests that WINs GaN processes and epitaxy growth is improving to the point where these effects can be considered second order for many applications.

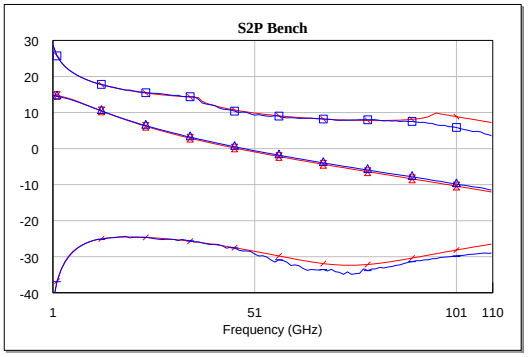


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*Fig.2; 1-110GHz Small Signal Model vs Measured Gmax, S21. S12 dB, for the 4x40um BF cell, 20V 100mA/mm (Model- red Meas-blue)*

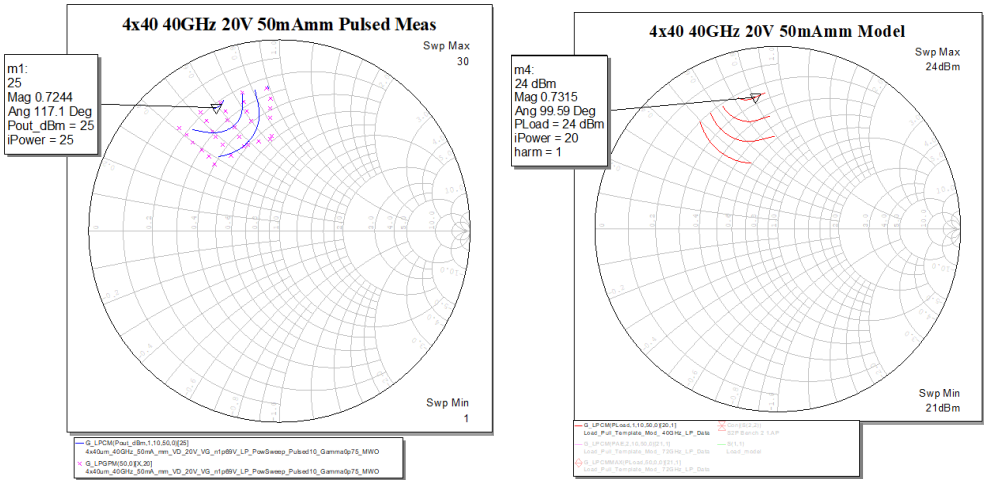



*Fig.3; 4x40umBF 40GHz, 20V 50mA.mm, a**)** Measured and b) model Contours of Pout dBm*

Power Sweeps Measured and Modelled

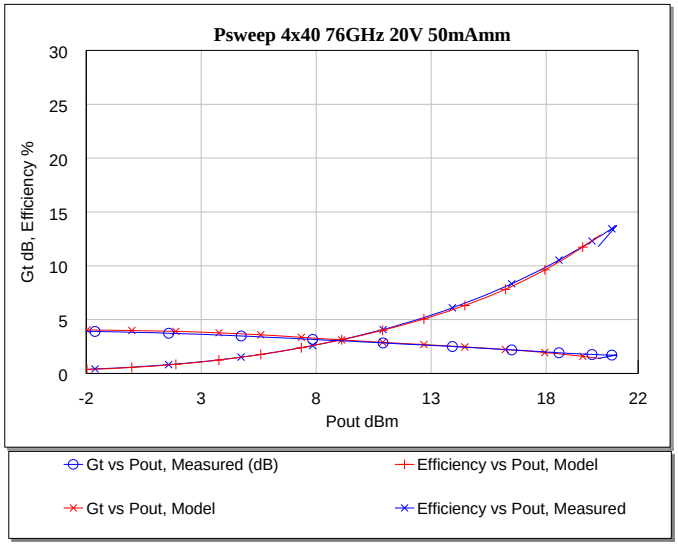



*Fig.4; 4x40um BF Measured vs Modelled 76GHz Power Sweep at Pmax load, Gt dB and Drain Efficiency % vs Pout dBm, 20V 50mA/mm*

Load pull contour results comparing modelled with measured are shown in Fig.3 for 76GHz, at 20V and 50mA/mm Idq, for a 4x40um cell. The load condition for the model simulation version has the same magnitude as the measured but is offset in phase to obtain a similar optimum performance point.

The 76GHz GHz power sweep gain and efficiency results are in good agreement with the measured data as in Fig.4. The modelled gain at low power is consistent with equivalent small signal measured data.

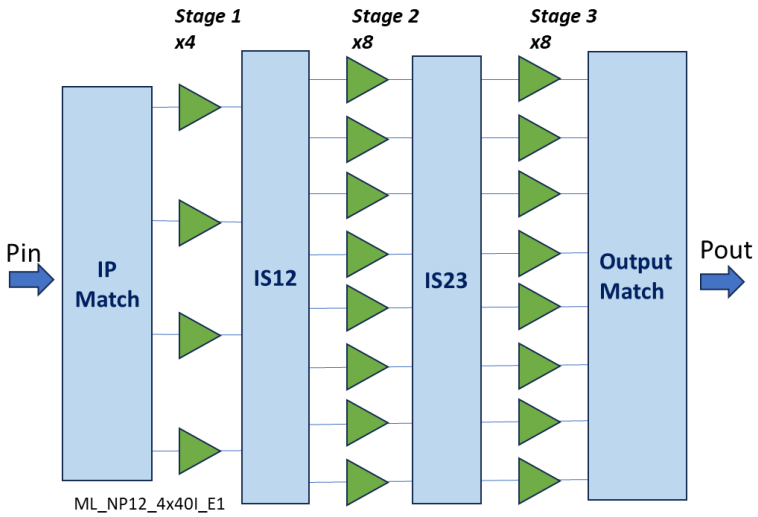
In terms of assisting the 71-76GHz amplifier design task the model replicates the load match gamma, effiency and gain compression verus swept power (at least under the measured conditions) well enough to be useful in making a first cut of a 71-76GHz HPA design.

2W E-band MMIC Design and Layout

Top Level Topology and Design Considerations

A number of circuit topologies were considered to achieve the target gain, power and size requirements. Based on the model performance a 3-stage design was selected for investigation with stage 1 consisting of 4 cells, and stages 2 and 3 being 8 cells each. Preliminary simulations suggested that this topology would meet the design specifications. Fig. 5 shows the top level topology and highlights the main passive matching blocks required for this implementation. These are Input Match, IS12 (Interstage Match 1 to 2), IS23 (Interstage Match 2 to 3), and Output Match.

*Fig.5; Top level HPA Topology*




To achieve a compact design, use of MIM caps is employed in the matching circuits. These can be quite small due to the high frequency of operation but are within the design rules of the NP12 process. An investigation was carried out to access the impact on performance due to tolerance variations of the MIM caps. This was completed on a 3-stage single cell test design and the results are illustrated in Fig.6. Tolerance was set to +/-5% for the simulations. The results show an acceptable level of performance variation due to tolerances on the MIM caps, and it is possible to apply design centring to reduce the sensitivity. Although this may be at the cost of some gain performance.

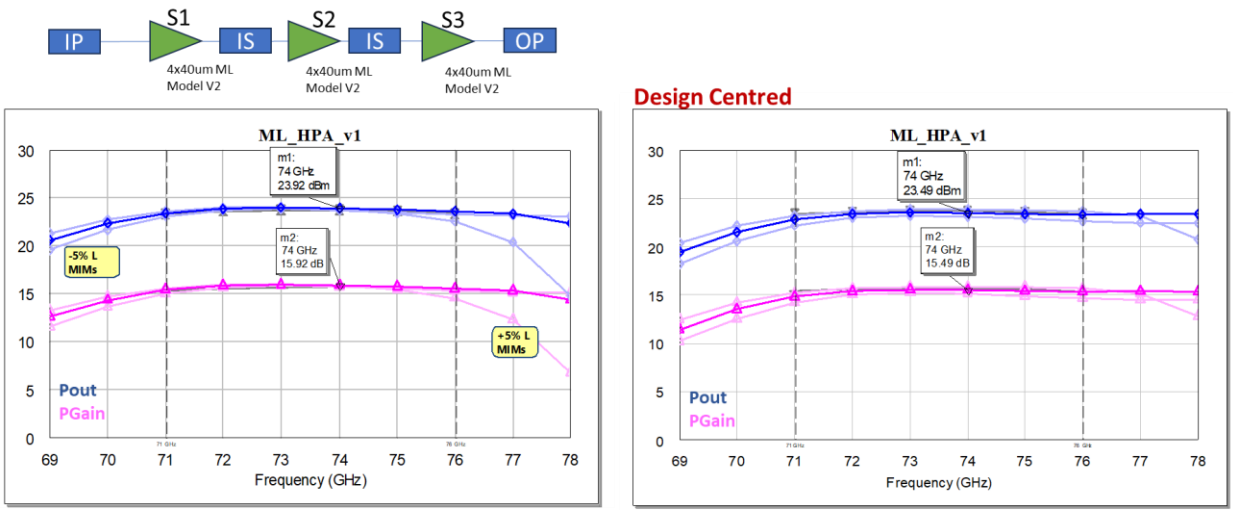



*Fig.6; MIM Cap tolerance analysis*

Another requirement for the design is for bias lines to be rated at 50% above process recommendation.

Output Match Design

The output array of cells are grouped into pairs, and the pairs are spaced further apart to facilitate better thermal performance and to allow room for internal decoupling on the interstage layouts.

The spacing dictates the combining structure for the output match circuit. A matching circuit has been designed using 2 shunt MIM caps close to the FET followed by a phase matched combining network to a single microstrip line and RF bond pad output. The output matching network is designed to present an optimum power match at the device plane for operation at E-Band.

Fig.7 shows the Axiem simulation layout of the critical section of the output match. This section is replicated at each cell on the output match. The rest of the output match is represented by PDK microstrip models and requires additional EM simulation to complete. However, as the critical section is captured by EM, the overall response will be representative.

Stage 3 drain bias lines are fed the from top and bottom side. RF Decoupling and a DC blocking capacitor are included. Resistive ties between array cells help prevent odd mode stability issues.

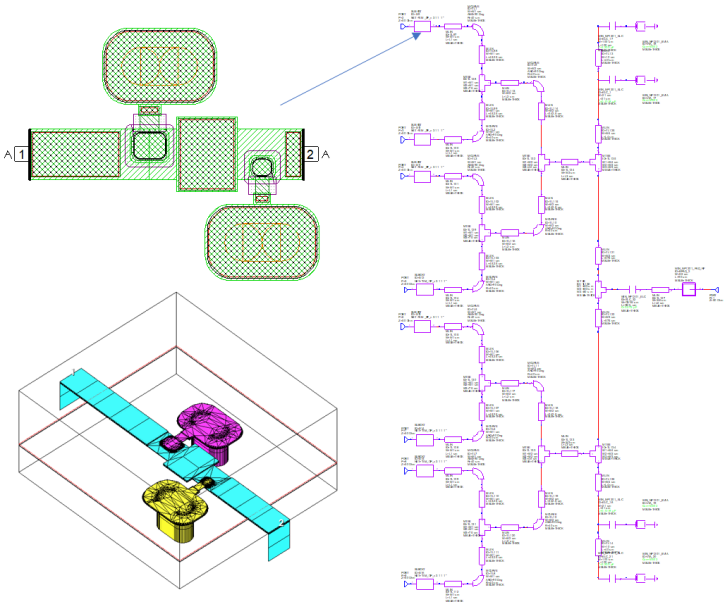


*Fig.7; Output Match*

Interstage 2-3 Design

Gain stages 2 and 3 consist of 8 cells each, therefore a 1:1 matching arrangement is used and replicated 8 times down the array. Decoupling capacitors and some small resistors are included at the intersections between matching circuits. Shared vias are used between the FET source and MIM caps. A full EM simualtion has been tuned in Axiem for this interstage match. A MIM cap is used for DC decoupling between drain and gate side.

Interstage 1-2 Design

Stage 1 consists of 4 cells, and is matched to the 8 cells of stage 2 by duplicating 4x 1:2 matching circuits. Shared vias are used between FET source via and MIM cap on the gate side of stage 2. A MIM cap is used for DC decoupling between drain and gate side. RF decoupling MIM caps are included between matching circuits in the array.

Input Match

The input match transformation is from 50 Ohms at the bond pad to optimum gain match at each of the 4 cells on stage 1 of the HPA. A MIM cap is used on the input for dc decoupling and RF decoupling is included on the bias feed lines.

Full HPA Simlation and layout

This section details the simulated results of the full HPA design using a combination of PDK elements and EM simulations where available. 20 instances of the MMIC-Lab 4x40um GaN HEMT model are used in the simulations and quiescent current is set to

100mA/mm (Vg=-1.69V), with drain current set to 20V.  A layout of the three stage PA is shown in Fig.8.

Narrow and wideband S-parameters are shown in Fig.9. A flat gain response is achieved with 18.2dB S21 at 74GHz. Input and output return loss is good, with better than 13dB achieved across the band.

Fig.10 shows a large signal power sweep at 74GHz. Saturated Power is 35dBm and peak PAE is 18%, with gain reduced from 18dB to 10dB in this condition.

Figs. 10b shows the large signal response verses frequency at gain compression of 5dB. At P5dB the output power is 33.4dBm with 13dB gain and 16% PAE.  Drain Current vs. Input Power simulation shows Id=0.677A at Pin=21dBm (P5dB).

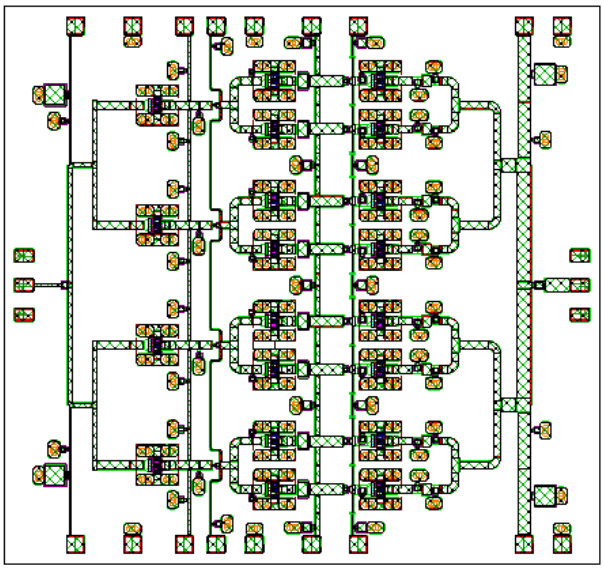


*Fig.8; Three stage E-band PA layout*

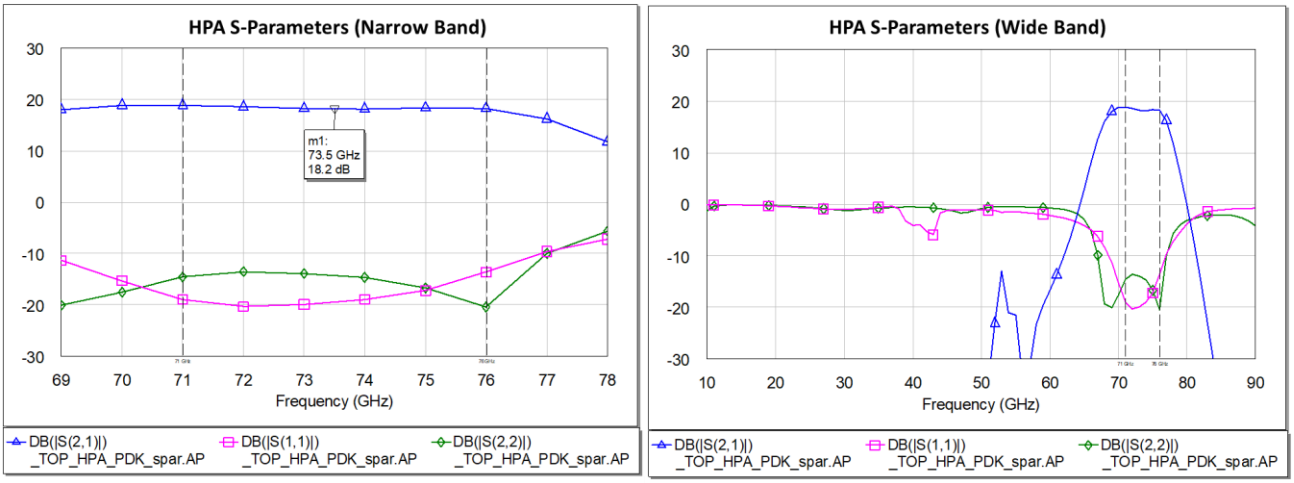



*Fig.9; S-parameter simulation*

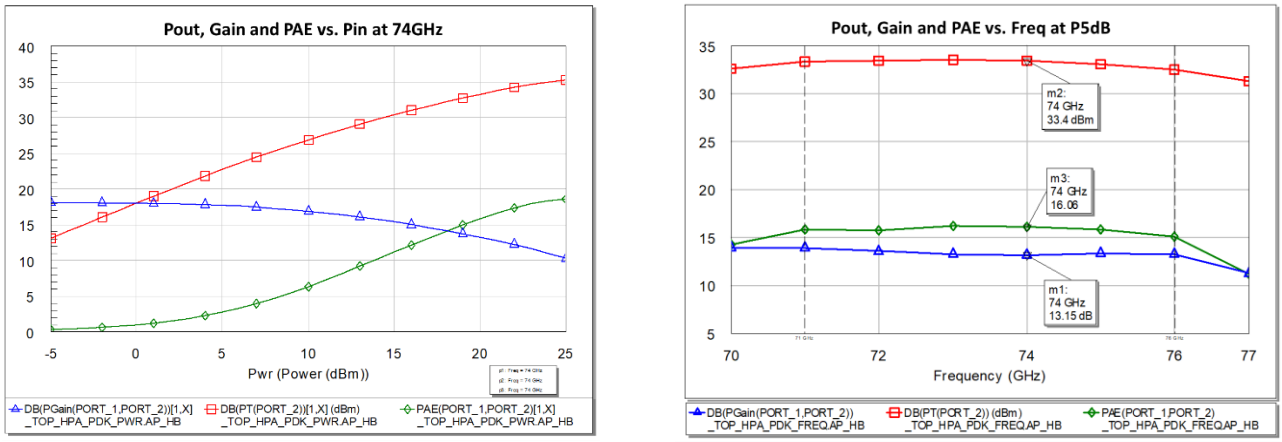



*Fig.10a; Large Signal simulation; Pout, Gain and PAE vs. Input Power and Fig.10b; P5dBv Gain and Power and PAE vs Frequency*

An internal stability analysis has been completed on the HPA across the full band using the Nyquist Stability Index criteria . Internal Gamma probes are inserted along the centre of the array at the gate and drain of each stage. Tuners are used to sweep the input and output impedances around the edge of the Smith chart. The 50 Ohm condition is shown in blue whith the swept impedance points in magenta. For stability the response should be -1<y<1. This condition is met on all responses. Stage 3 gate stability is marginal at 83GHz and should be investigated further.

## Conclusions and Future Work

A preliminary design for a 71-76GHz MMIC on WIN GaN NP12 is presented. The design work is based on a measurement extracted non-linear model for a 4x40um butterfly layout unit cell. Detailed design of each matching stage has been completed using passive PDK models, with EM simulations for critical elements and subsections. The HPA achieves 33dBm output power at P5dB with 16% PAE and 13dB gain, and is in line with initial requirements. The design is stable using Stability Index simulations with internal Gamma probes. A preliminary layout for the MMIC is presented.

The work shows that a 71-76GHz HPA on NP12 is feasible.

Some further work is required to prepare the design for final tape-out. This would include EM simulation and tuning of the remaining passive sub-sections, integrated EM simulations, further stability analysis using NDF (Normalised Determinant Function). Thermal analysis at FET model level can be included and accessed in the RF simulation and full FEM Thermal analysis of the MMIC could be investigated.